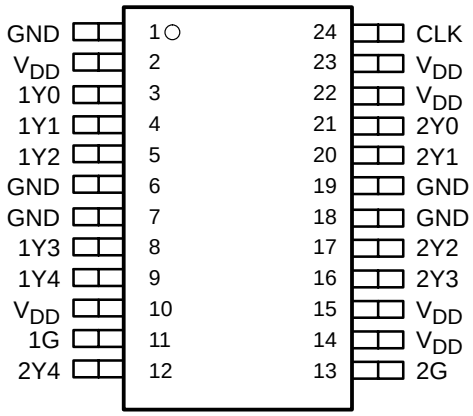
- **High Performance 1:10 Clock Driver for General Purpose Applications. Operates up to 200 MHz at V_{DD} 3.3 V**
- **Pin-to-Pin Skew < 100 ps at V_{DD} 3.3 V**
- **V_{DD} Range: 2.3 V to 3.6 V**
- **Operating Temperature Range –40°C to 85°C**
- **Output Enable Glitch Suppression**
- **Distributes One Clock Input to Two Banks of Five Outputs**
- **25-Ω On-Chip Series Damping Resistors**
- **Packaged in 24-Pin TSSOP**

PW PACKAGE
(TOP VIEW)

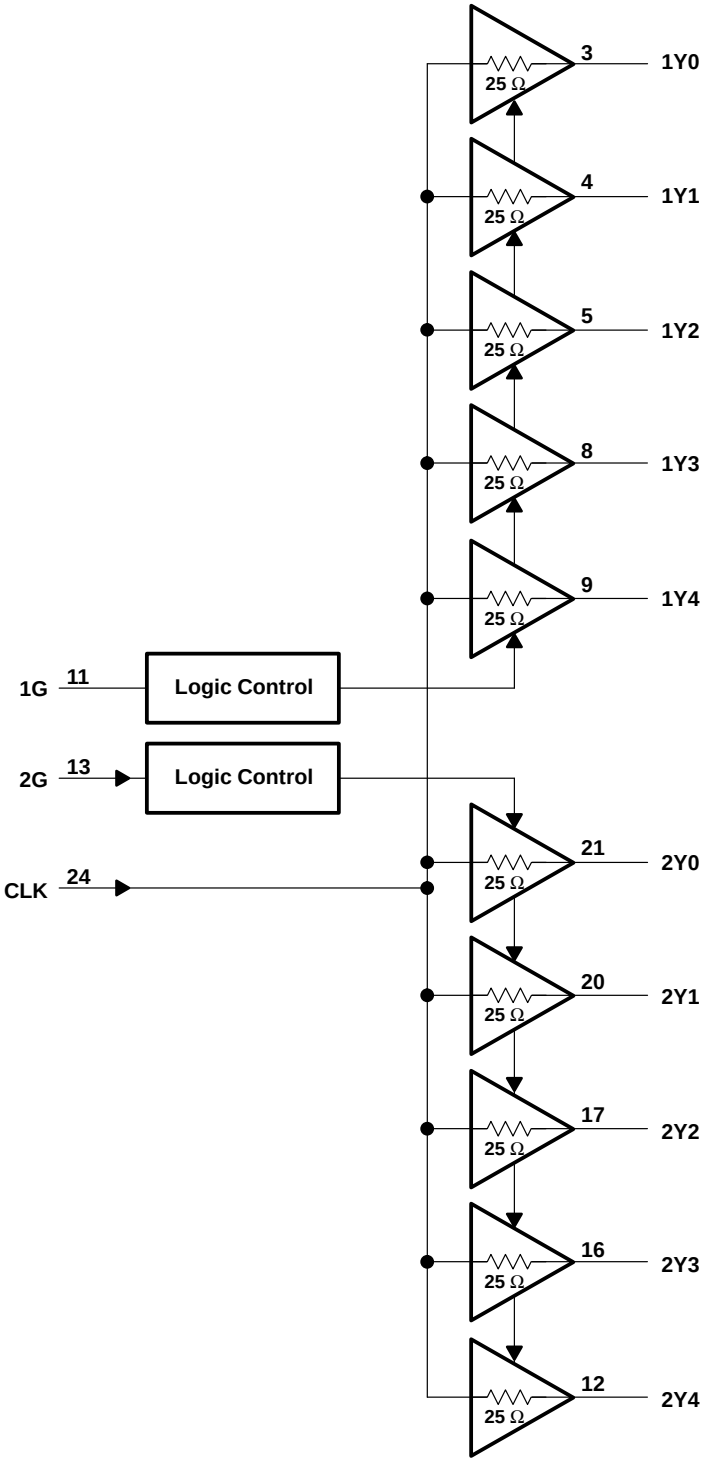


description

The CDCVF2310 is a high-performance, low-skew clock buffer that operates up to 200 MHz. Two banks of five outputs each provide low-skew copies of CLK. Through the use of the control pins 1G and 2G, the outputs of bank 1Y(0:4) and 2Y(0:4) can be placed in a low state regardless of the CLK input. The device operates in a 2.5-V and 3.3-V environment. The built-in output enable glitch suppression ensures a synchronized output enable sequence to distribute full period clock signals.

The CDCVF2310 is characterized for operation from –40°C to 85°C.

functional block diagram



The 1G and 2G output enables are active high. For example, if the 1G pin is logic high, the 1Y(0:4) outputs will follow the input CLK. If 1G is logic low, the 1Y(0:4) outputs will drive low, independent of the state of the input clock.

FUNCTION TABLE

INPUT			OUTPUT	
1G	**2G**	**CLK**	**1Y(0:4)**	**2Y(0:4)**
L	L	X	L	L
H	L	H	H	L
L	H	H	L	H
H	H	H	H	H

Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	**NO.**		
1G	11	I	Output enable control for 1Y(0:4) outputs. This output enable is active high meaning the 1Y(0:4) clock outputs will follow the input clock (CLK) if this pin is logic high. If this pin is logic low, the 1Y(0:4) outputs will drive low independent of the state of CLK.
2G	13	I	Output enable control for 2Y(0:4) outputs. This output enable is active high meaning the 2Y(0:4) clock outputs will follow the input clock (CLK) if this pin is logic high. If this pin is logic low, the 2Y(0:4) outputs will drive low independent of the state of CLK.
1Y[0:4]	3, 4, 5, 8, 9	O	Buffered output clocks
2Y(0:4)	21, 20, 17, 16, 12	O	Buffered output clocks
CLK	24	I	Input reference frequency
GND	1, 6, 7, 18, 19		Ground
V_{DD}	2, 10, 14, 15, 22, 23	Power	DC power supply, 2.3 V – 3.6 V

detailed description

output enable glitch suppression circuit

The purpose of the glitch suppression circuitry is to ensure the output enable sequence is synchronized with the clock input such that the output buffer will be enabled on the next full period of the input clock (negative edge triggered by the input clock). The G input must be stable one t_{en} – time prior to the falling edge of the CLK for predictable operation.

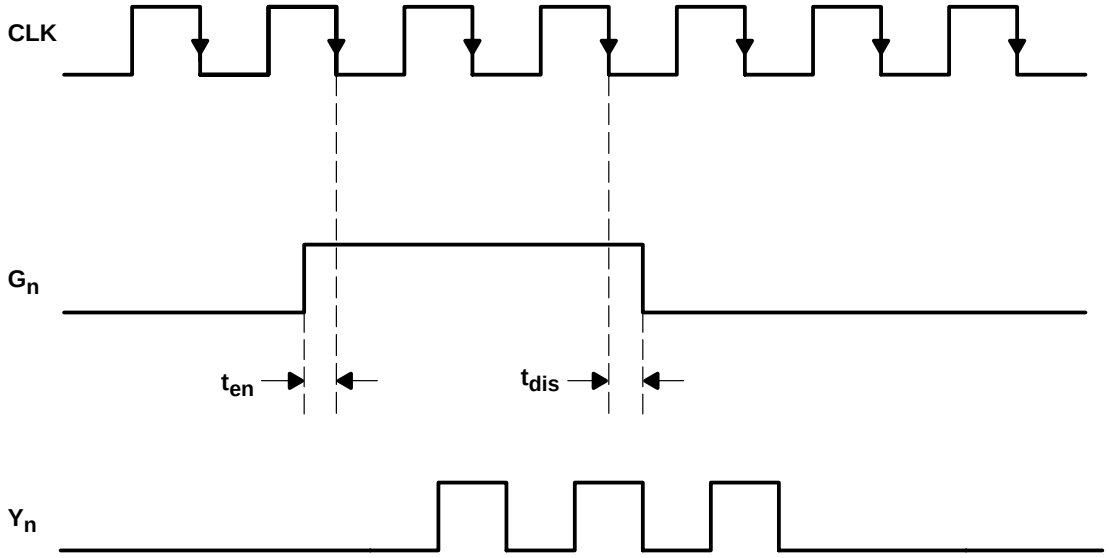


Figure 1. G (t_{en}, t_{dis}) Relative to CLK↓

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{DD} . . . . . –0.5 V to 4.6 V
Input voltage range, V_I (see Notes 1 and 2) . . . . . –0.5 V to V_{DD} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) . . . . . –0.5 V to V_{DD} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD}) . . . . . ±50 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD}) . . . . . ±50 mA
Continuous total output current, I_O (V_O = 0 to V_{DD}) . . . . . ±50 mA
Package thermal impedance, θ_{JA} (see Note 3): PW package . . . . . 120°C/W
Storage temperature range T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		2.3	2.5		V
			3.3	3.6	
Low-level input voltage, V_{IL}	V_{DD} = 3 V to 3.6 V			0.8	V
	V_{DD} = 2.3 V to 2.7 V			0.7	
High-level input voltage, V_{IH}	V_{DD} = 3 V to 3.6 V	2			V
	V_{DD} = 2.3 V to 2.7 V	1.7			
Input voltage, V_I		0		V_{DD}	V
High-level output current, I_{OH}	V_{DD} = 3 V to 3.6 V			–12	mA
	V_{DD} = 2.3 V to 2.7 V			–6	
Low-level output current, I_{OL}	V_{DD} = 3 V to 3.6 V			12	mA
	V_{DD} = 2.3 V to 2.7 V			6	
Operating free-air temperature, T_A		–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IK}	Input voltage	V_{DD} = 3 V,	I_I = –18 mA			–1.2	V
I_I	Input current	V_I = 0 V or V_{DD}				±5	μA
I_{DD}†	Static device current	CLK = 0 V or V_{DD},	I_O = 0 mA, V_{DD} = 3.3 V			25	μA
C_I	Input capacitance	V_{DD} = 2.3 V to 3.6 V,	V_I = 0 V or V_{DD}		2.5		pF
C_O	Output capacitance	V_{DD} = 2.3 V to 3.6 V,	V_I = 0 V or V_{DD}		2.8		pF

† For I_{DD} over frequency see Figure 5.

V_{DD} = 3.3 V ±0.3 V

PARAMETER		TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{OH}	High-level output voltage	V_{DD} = min to max,	I_{OH} = –100 μA	V_{DD} – 0.2			V
		V_{DD} = 3 V	I_{OH} = –12 mA	2.1			
			I_{OH} = –6 mA	2.4			
V_{OL}	Low-level output voltage	V_{DD} = min to max,	I_{OL} = –100 μA			0.2	V
		V_{DD} = 3 V	I_{OL} = 12 mA			0.8	
			I_{OL} = 6 mA			0.55	
I_{OH}	High-level output current	V_{DD} = 3 V,	V_O = 1 V	–28			mA
		V_{DD} = 3.3 V,	V_O = 1.65 V		–36		
		V_{DD} = 3.6 V,	V_O = 3.135 V			–14	
I_{OL}	Low-level output current	V_{DD} = 3 V,	V_O = 1.95 V	28			mA
		V_{DD} = 3.3 V,	V_O = 1.65 V		36		
		V_{DD} = 3.6 V,	V_O = 0.4 V			14	

‡ All typical values are at respective nominal V_{DD}.

V_{DD} = 2.5 V ±0.2 V

PARAMETER		TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{OH}	High-level output voltage	V_{DD} = min to max,	I_{OH} = –100 μA	V_{DD} – 0.2			V
		V_{DD} = 2.3 V	I_{OH} = –6 mA	1.8			
V_{OL}	Low-level output voltage	V_{DD} = min to max,	I_{OL} = 100 μA			0.2	V
		V_{DD} = 2.3 V	I_{OL} = 6 mA			0.55	
I_{OH}	High-level output current	V_{DD} = 2.3 V,	V_O = 1 V	–17			mA
		V_{DD} = 2.5 V,	V_O = 1.25 V		–25		mA
		V_{DD} = 2.7 V,	V_O = 2.375 V			–10	
I_{OL}	Low-level output current	V_{DD} = 2.3 V,	V_O = 1.2 V	17			mA
		V_{DD} = 2.5 V,	V_O = 1.25 V		25		
		V_{DD} = 2.7 V,	V_O = 0.3 V			10	

‡ All typical values are at respective nominal V_{DD}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

			MIN	NOM	MAX	UNIT
f_{clk}	Clock frequency	V_{DD} = 3 V to 3.6 V	0		200	MHz
		V_{DD} = 2.3 V to 2.7 V	0		170	

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

V_{DD} = 3.3 V ±0.3 V (see Figure 2)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH} / t_{PHL}	CLK to Yn (see Figure 2)	f = 0 MHz to 200 MHz	1.3		2.8	ns
$t_{sk(o)}$	Output skew (Yn to Yn) (see Note 4 and Figure 4)				100	ps
$t_{sk(p)}$	Pulse skew (see Figure 5)				250	ps
$t_{sk(pp)}$	Part-to-part skew				500	ps
t_r	Rise time (see Figure 3)	V_O = 0.4 V to 2 V	0.7		2	V/ns
t_f	Fall time (see Figure 3)	V_O = 2 V to 0.4 V	0.7		2	V/ns
t_{en}	G before CLK ↓ (see Figure 1)	$V_{(threshold)} = V_{DD}/2$	0.1			ns
t_{dis}	G after CLK ↓ (see Figure 1)		0.4			

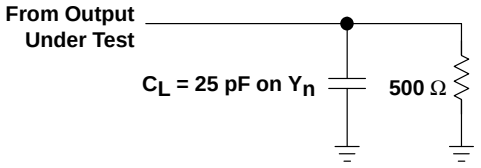
† All typical values are at respective nominal V_{DD}.
NOTE 4: The $t_{sk(o)}$ specification is only valid for equal loading of all outputs.

V_{DD} = 2.5 V ±0.2 V (see Figure 2)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH} / t_{PHL}	CLK to Yn (see Figure 2)	f = 0 MHz to 170 MHz	1.5		3.5	ns
$t_{sk(o)}$	Output skew (Yn to Yn) (see Note 4 and Figure 4)				170	ps
$t_{sk(p)}$	Pulse skew (see Figure 5)				400	ps
$t_{sk(pp)}$	Part-to-part skew				600	ps
t_r	Rise time (see Figure 3)	V_O = 0.4 V to 1.7 V	0.5		1.4	V/ns
t_f	Fall time (see Figure 3)	V_O = 1.7 V to 0.4 V	0.5		1.4	V/ns
t_{en}	G before CLK ↓ (see Figure 1)	$V_{(threshold)} = V_{DD}/2$	0.1			ns
t_{dis}	G after CLK ↓ (see Figure 1)		0.4			

† All typical values are at respective nominal V_{DD}.
NOTE 4: The $t_{sk(o)}$ specification is only valid for equal loading of all outputs.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 200 MHz, Z_O = 50 Ω, t_r < 1.2 ns, t_f < 1.2 ns.

Figure 2. Test Load Circuit

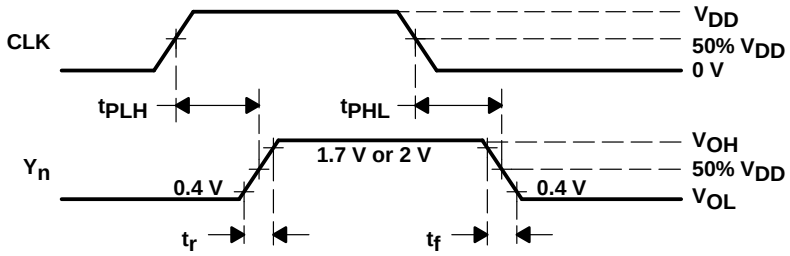


Figure 3. Voltage Waveforms Propagation Delay Times

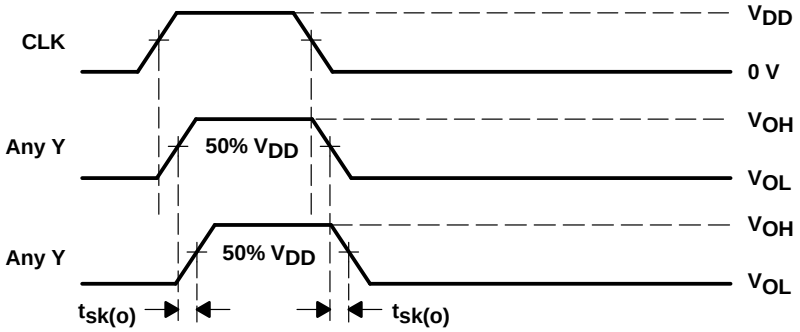
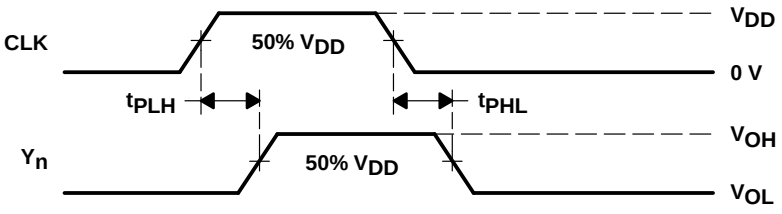


Figure 4. Output Skew



NOTE: $t_{sk(p)} = | t_{PLH} - t_{PHL} |$

Figure 5. Pulse Skew

PARAMETER MEASUREMENT INFORMATION

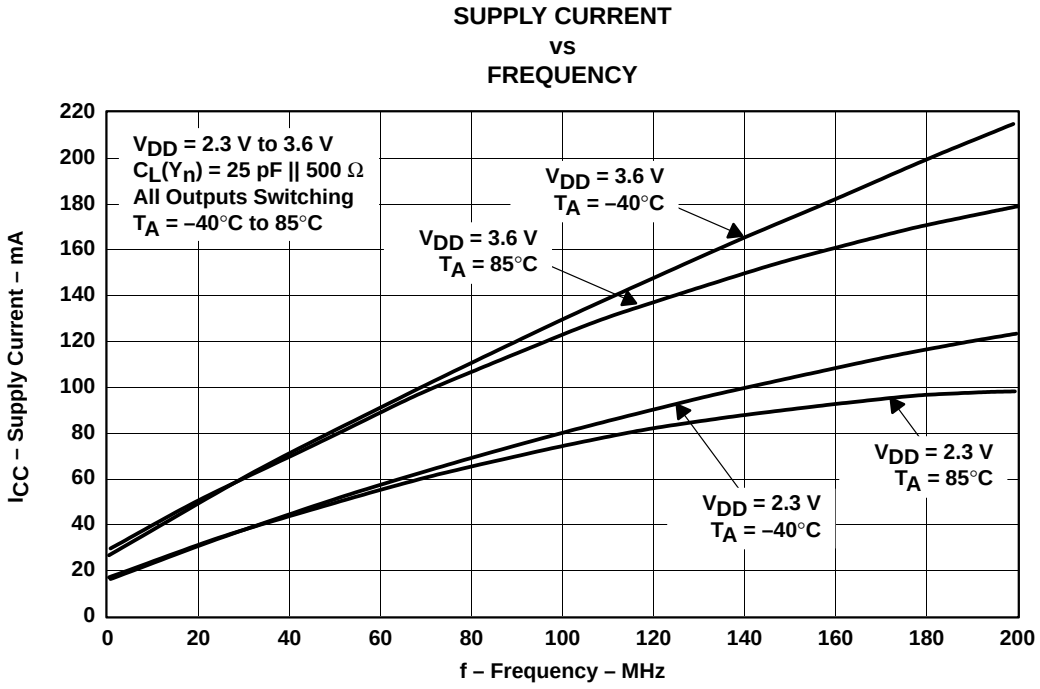
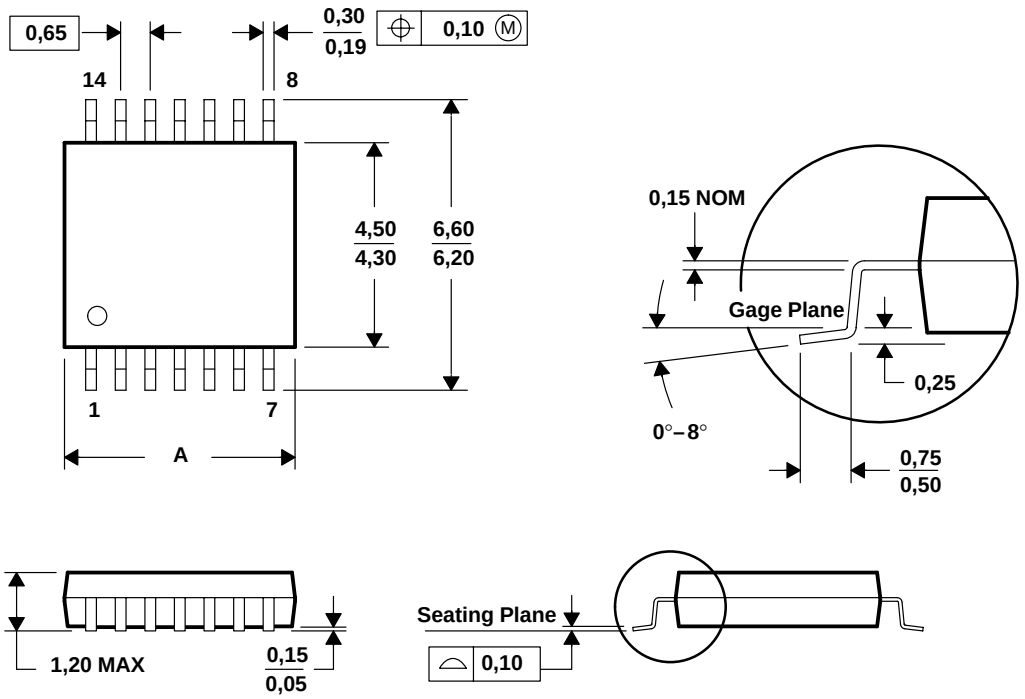


Figure 6

MECHANICAL DATA

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265